IN THE SPECIFICATION

Please replace the paragraph beginning at line 21, page 5 and ending at line 20, page 6 with the following rewritten paragraph:

Figure 2 illustrates an embodiment of the present invention of a receiver 103 configured to receive serial data 201 transmitted from transmitter 101 through medium 102, e.g., wired, wireless. Receiver may comprise a phase detector 202 configured to receive serial data 201 transmitted by transmitter 101 through medium 102, e.g., wired, wireless. Phase detector 202 may further be configured to generate N synchronization states that are inputted to retiming mechanism 205. Phase detector 202 may further be configured to generate an error signal. The functionality of phase detector 202 is described in greater detail in U.S. Publication No. 20020085657, filed on December 28, 2000, entitled "Multiphase Clock Recovery Using D-Type Phase Detector," which is hereby incorporated herein by reference in its entirety. The error signal generated by phase detector 202 is filtered through filter 203 which outputs a control voltage used by oscillator 204, e.g., voltage controlled oscillator, to generate N phases of a clock that is inputted to retiming mechanism 205. In one embodiment, oscillator 204 may be configured to operate at a frequency lower than the serial data rate thereby saving power. The output of oscillator 204 is also inputted to phase detector 202 as illustrated in Figure 2. Additional details regarding the functionality of oscillator 204 is described in related U.S. Application Serial Nos. 09/726,282 and 09/726,285, both filed on November 30, 2000, which are hereby incorporated herein by reference in their entirety. Phase detector 202, filter 203 and oscillator 204, e.g., voltage controlled oscillator, may collectively be referred to as a clock and data recovery unit configured to extract a clock from the serial data stream 201 which is used to retime the data, i.e., diminish jitter, by retiming mechanism 205 as described in the description of Figures 4-8. The clock and data recovery unit is described in greater detail in U.S. Patent

No. 6,441,667, issued on August 27, 2002, entitled "Multiphase Clock ~~Generation~~ Generator," which is hereby incorporated herein by reference in its entirety.